



**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re application of: Nikhil Vishwanath Kelkar

Attorney Docket No.: NSC1P300/P05882

Application No.: 10/824,903

Examiner: Shankle, A.

Filed: April 14, 2004

Group: 2891

Title: WAFER LEVEL PACKAGE DESIGN  
THAT FACILITATES TRIMMING AND  
TESTING

Confirmation No: 7593

**CERTIFICATE OF MAILING**

I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as first-class mail on July 12, 2006 in an envelope addressed to the Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450.

Signed: \_\_\_\_\_

*Laura M. Dean*  
Laura M. Dean

**INFORMATION DISCLOSURE STATEMENT  
BEFORE FINAL ACTION OR NOTICE OF ALLOWANCE  
(37 CFR §§ 1.56 AND 1.97(c))**

Mail Stop Amendment  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Dear Sir:

The references listed in the attached PTO Form 1449, a copy of which is attached, may be material to examination of the above-identified patent application. Applicants submit this reference in compliance with their duty of disclosure pursuant to 37 CFR §§1.56 and 1.97. The Examiner is requested to make this citation of official record in this application.

This Information Disclosure Statement is not to be construed as a representation that a search has been made, that additional information material to the examination of this application does not exist, or that this reference indeed constitutes prior art.

This Information Disclosure Statement is being filed after the mailing date of the first Office Action on the merits, or after three months of the filing date of this application, whichever event occurred last, but it is believed before the mailing date of either: (i) a final action under §1.113 or (ii) a notice of allowance under §1.311, whichever occurs first.

07/17/2006 GWORDOF1 00000069 10824903

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180.00 DP

Accompanying this Information Disclosure Statement is

☐ a statement as specified in 37 CFR 1.97(e); or

☒ the fee set forth in 37 CFR 1.17(p).

If fees are due, enclosed is our Check No. 30646 for \$180.00 in payment of the Information Disclosure Statement Fee. If it is determined that any additional fees are due, the Commissioner is hereby authorized to charge such fees to Deposit Account 500388 (Order No. NSC1P300).

Respectfully submitted,

BEYER WEAVER & THOMAS, LLP



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Form 1449 (Modified)	Atty Docket No. NSC1P300/P05882	Application No.: 10/824,903
<b>Information Disclosure Statement By Applicant</b>	Applicant: Kelkar	
(Use Several Sheets if Necessary)	Filing Date 04/14/2004	Group 2891

### U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
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Examiner				Date Considered			

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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	Applicant:	
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	Filing Date	Group
	04/14/2004	2891

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**Other Documents**

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
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	C2	Kulicke & Soffa, Flip Chip Division, Polymer Collar™ Wafer Level Package, "See the Polymer Collar™ WLP Difference!", December 7, 2001, www.kns.com.
	C3	Lau et al., "Chip Scale Package: Design, Materials, Process, Reliability, and Applications," February 28, 1999, McGraw-Hill Professional Publishing; Chapter 1, pages 1-41.
	C4	Rao R. Tummala, "Fundamentals of Microsystem Packaging," May 8, 2001, McGraw-Hill Professional Publishing; Chapters 2, 10 and 17.
	C5	"Polymer Collar WLP™, Wafer Level Package Family", © 2002, downloaded from <a href="http://www.kns.com/prodserv/PDFS/PCD/polymer_collar.pdf">www.kns.com/prodserv/PDFS/PCD/polymer_collar.pdf</a> , 2 pages.
	C6	"Presenting Polymer Collar WLP™ – A New Wafer Level Package for Improved Solder Joint Reliability", © 2002, downloaded from <a href="http://www.kns.com/prodserv/flipchip/pdf/PC_ad.pdf">www.kns.com/prodserv/flipchip/pdf/PC_ad.pdf</a> , 1 page.
	C7	Barrett et al., Kulicke & Soffa, "Polymer Collar WLP™ – A New Wafer Level Package for Improved Solder Joint Reliability", © 2002, downloaded from <a href="http://www.kns.com/resources/articles/PolymerCollar.pdf">www.kns.com/resources/articles/PolymerCollar.pdf</a> , 9 pages.
	C8	Bogatin, Eric, "All Dressed Up and Nowhere to Go"; Semiconductor International, May 1, 2002, downloaded December 23, 2003, from <a href="http://www.reed-electronics.com/semiconductor/index.asp?layout=article@articleid=CA213812@rid=0&amp;rme=0&amp;cfd=1">www.reed-electronics.com/semiconductor/index.asp?layout=article@articleid=CA213812@rid=0&amp;rme=0&amp;cfd=1</a> , 2 pages.
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Examiner		Date Considered

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**Other Documents**

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
	C10	U.S. Patent Application 10/080,913, filed February 21, 2002.
	C11	U.S. Patent Application 10/224,291, filed August 19, 2002.
	C12	U.S. Patent Application 10/707,208, filed November 26, 2003.
Examiner		Date Considered

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